



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

BOYLAN et al.

Atty. Ref.: 922-143; Confirmation No. 4519

Appl. No. 09/919,806

TC/A.U. 2188

Filed: August 2, 2001

Examiner: J.A. Lane

For: AUTOMATIC GENERATION OF INTERCONNECT  
COMPONENTS

\* \* \* \* \*

October 25, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**RESPONSE**

In response to the Office Action mailed 07/29/2004, the following remarks are submitted.

The Examiner has requested the identity of any prior art known to the applicant (or other substantively involved in the preparation or prosecution of this application) of prior art that could reasonably be used in a prior art-based rejection of the pending claims. Bearing in mind that the request does not require applicant to perform a search of any kind, the undersigned made this query to the UK agent providing instructions for prosecution. That response is quoted below:

“I am in a little difficulty in providing an exhaustive answer to the Examiner’s request because the chip design group at Galway was disbanded two years ago and all the inventors left the assignee’s employment at that time. However I have reviewed the original GB file and the source documents (as the inventors’ internal ‘invention disclosure form’) and have not found any reference to prior art or any search for it. The invention as particularly described employs a known hardware design language (Verilog) but I do not think that is what the Examiner has in mind (and in any case the

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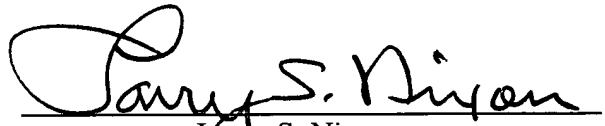
specification makes this clear throughout). So far as I am aware feature (b) in claim 1 was a novel design constraint, which is clear from the inventors' notes."

There being no other outstanding request or ground of rejection, this entire application is now believed to be in allowable condition and a formal Notice to that effect is respectfully solicited.

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

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